REMARKS/ARGUMENTS

Reconsideration of this application is requested. Claims 1-9 remain active in the case. The independent claim 1 have been amended in order to more particularly point out and distinctly claim that which applicants regard as their invention. No new matter is introduced.

Claims 1-10 were rejected under 35 U.S.C. 102(b) for reason of record that can be found on pages 2-3 in the Office action identified above, which is Part of Paper No./Mail Date 20040830.

To overcome the 102 rejections, claim 1 has been amended. Haspeslagh (US 2003/0006450) teaches a non-volatile electrically erasable and programmable memory structure including stripes of contiguous poly lines, alternately formed in one of two poly-layers. In order to form the stripes of contiguous poly lines, a chemical-mechanical-polishing is essential and is carried out after the deposition of the second poly-layer. In this manner, a non-volatile electrically erasable and programmable memory array having parallel poly lines is fabricated.

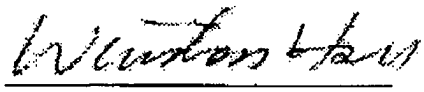
According to Haspeslagh, to program a bit of a cell of the memory array underneath a specific poly line, for example, referring to Fig.5 of US 2003/0006450, the word line 5 (W_5), the contiguous poly lines W_1~W_3 on the left side of the cell are biased at a voltage that is large enough to invert that part of the channel underneath these poly lines thereby creating a virtual source to the FET structure of poly line W_4. The poly lines W_5~W_9 are biased at a voltage that is large enough to invert that part of the channel underneath these poly lines thereby creating a virtual drain to the FET structure of poly line W_4. The voltage applied to poly lines W_5~W_9 has to be higher than the voltage applied to the drain (13).

Haspeslagh teaches away from that "when programming a memory cell defined by a specific row of said word lines of said electrically programmable non-volatile memory

array, only two columns of said assistant gates next to said memory cell are biased to a voltage V_i that is sufficient to correspondingly induce two columns of inversion regions", as required by the amended claim 1. Further, Haspeslagh does not teach the limitation that "rows of word lines intersecting said columns of assistant gates", as required by the amended claim 1. Besides, applicants respectfully submit that Haspeslagh does not teach "at least one end of each said columns of assistant gates partially overlaps with a doped pickup well formed in said semiconductor substrate, and wherein a bit line voltage is provided to said doped pickup well", as required by the amended claim 1. Accordingly, reconsideration of the amended claim 1 is politely requested.

As Claims 2-9 are dependent upon claim 1, they should be allowable if claim 1 is allowed. Reconsideration of claims 2-9 is politely requested. Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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